AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 3, line 13 with the following amended paragraph:

-- In a somewhat different approach discussed in the U.S. patent application serial No. ~~09/349,086~~ 09/349,087 (Roberts), entitled "Mapping Arbitrary Signals into SONET", filed on July 8, 1999 and assigned to Nortel Networks Limited, arbitrary electrical signals are converted into SONET optical signals by using a synchronizer. The synchronizer maps the arbitrary electrical signals into SONET signals such that the electrical signals can be recovered with low timing jitter at low cost at the far end. This mapping method can be used for tributaries of almost any continuous format. The synchronizer recognizes selected protocols, frames on them, and effects the corresponding performance monitoring.--

Please replace the paragraph beginning at page 5, line 1 with the following amended paragraph:

-- According to a second broad aspect of the invention, there is provided a desynchronizer for reverse mapping a frame received over a data network into an electrical digital signal having an arbitrary transmission rate. The desynchronizer includes a clock recovery unit, a reverse mapping unit and a data transmitter unit. The clock recovery unit receives the frame and recovers therefrom a data clock signal indicative of a line transmission rate. The reverse mapping unit extracts from the frame a stream of data bits according to a reverse mapping algorithm, on the basis of the line transmission rate. The data transmitter unit transmits the extracted stream of data bits on a basis of both the line transmission rate and the arbitrary transmission ~~rates~~ rate, for generating an electrical digital signal

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characterized by the arbitrary transmission rate. --

Please replace the paragraph beginning at page 8, line 4 with the following amended paragraph:

-- Figure 2 is a functional block diagram of the synchronizer 106 that receives an electrical digital signal S at input 200. The synchronizer 106 comprises a data recovery unit 202 that is operative to extract from the signal S a stream of data bits and a data clock signal, hereinafter referred to as the first data clock signal. This first data clock signal is indicative of the arbitrary transmission rate R for the signal S. As shown in Figure 2, the data recovery unit 202 includes a receiver 212 and a flexible clock recovery circuit 214. The flexible clock recovery circuit 214 is capable of clock recovery over a broad continuous range of bit-rates. An example of such a circuit is disclosed in the Canadian patent application filed on November 10, 1999 and published on June 22, 2000, entitled "Apparatus and Method for Versatile Digital Communication", by Habel et al., assigned to Northern Telecom Limited. --

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Please replace the paragraph beginning at page 8, line 29 with the following amended paragraph:

-- In a specific, non-limiting example of implementation, the clock generator unit 204 includes a multiplier ~~206~~ 216 that implements frequency multiplication for generating the second data clock signal, and an input 208 for receiving a control signal. In particular, the multiplier ~~206~~ 216 is operative to multiply the first data clock signal up to a second data clock signal that is indicative of a line transmission rate ~~that is compatible with a line~~ that falls within the range of allowable transmission ~~rate~~ rates for ~~of~~ the network 102. The control signal received at input 208 is generated by a frequency control unit 210 that automatically controls the multiplier ~~206~~ 216. --

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Please replace the paragraph beginning at page 9, line 9 with the following amended paragraph:

-- The automatic frequency control unit 210 is operative to detect the incoming arbitrary transmission rate for the signal and~~, on the basis of a pre-defined desired line transmission rate~~ to automatically set the multiplier ~~206~~ 216 such that ~~the~~ an appropriate frequency multiplication is applied to the first data clock signal for increasing the latter to the second data clock signal. The automatic frequency control unit 210 sets the multiplier 216 on the basis of a pre-defined and desired line transmission rate, whereby, after multiplication, the second data clock signal is indicative of this pre-defined line transmission rate. In an alternative, the frequency control unit 210 is itself controlled by a system operator and receives provisioning information, such as a ~~the~~ desired line transmission rate, from the system operator. The well documented concept of frequency multiplication is well known to those skilled in the art and, as such, will not be described in further detail. --

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Please replace the paragraph beginning at page 9, line 22 with the following amended paragraph:

-- The second data clock signal is passed from the clock generator unit 204 to a mapping unit 206. The mapping unit 206 is responsible for mapping the stream of data bits into a DS3 frame for transmission over the asynchronous electrical DS3 network 102, on a basis of the second data clock signal. Thus, the mapping algorithm is independent of the format and bit rate of the network 102 in the sense that the line transmission rate is recovered from the first data clock signal of the incoming digital signal S, since the clock generator 204 processes the first data clock signal to generate the second data clock signal. This is contrary to existing mapping systems in which the line transmission rate is recovered from a local clock reference of the network 102. --

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Please replace the paragraph beginning at page 13, line 22 with the following amended paragraph:

-- The data clock signal indicative of the line transmission rate and the stream of data bits, including stuff bits, are input to a reverse mapping unit 404. The reverse mapping unit 404 includes a time slot interchange unit 412 and a demultiplexer 414 for extracting ~~the OCO and FEC~~ Optical Channel Overhead (OCO) and Forward Error Correction (FEC) information from the corresponding timeslots on a basis of the recovered data clock signal indicative of the line transmission rate. The reverse mapping unit 404 further includes a reverse mapper 416 for reverse mapping the stream of data bits extracted from the wrapped DS3 frame, on a basis of the particular mapping algorithm implemented at the synchronizer 106. --

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